

CLAIMS

What is claimed is:

- 1 1. A FLASH controller comprising:
2 a USB interface unit, wherein USB interface unit implements a USB standard
3 that has a bus speed equal or greater than 12 Mb/s;
4 an internal bus coupled to the USB interface unit; and
5 a FLASH interface unit coupled to the internal bus, the FLASH interface unit
6 includes FLASH controller logic that allows the throughput for access to a FLASH memory to
7 match the speed of the USB standard.
- 1 2. The FLASH controller of claim 1 wherein the USB standard comprises the
2 USB 2.0 standard.
- 1 3. The FLASH controller of claim 1 wherein the software program for the FLASH
2 controller is stored along with data in at least one of the plurality of FLASH
3 memories for cost reduction and field upgrade ability.
- 1 4. The FLASH controller of claim 1 wherein the throughput for access to a
2 FLASH memory to match the speed of the USB standard is accomplished by providing a wider
3 bandwidth FLASH data bus.
- 1 5. The FLASH controller of claim 1 wherein the throughput for access to a

FLASH memory to match the speed of the USB standard is accomplished by providing concurrent internal and external read and write cycles.

6. The FLASH controller of claim 4 wherein the wider data bandwidth is provided by using a FLASH memory with the appropriate data width.

7. The FLASH controller of claim 4 wherein the wider data bandwidth is provided by using multiple FLASH memories.

8. The FLASH controller of claim 1 wherein the throughput for access to a FLASH memory to match the speed of the USB standard is accomplished by providing a wider bandwidth FLASH data bus and concurrent internal and external read and write cycles.

9. The FLASH controller of claim 1 including a FLASH type detection algorithm for determining if a FLASH type is supported by the FLASH controller.

10. The FLASH controller of claim 1 wherein an external power regulator, reset circuit and crystal are integrated via mixed signal technology or Multi-Chip package.

11. A mass storage device comprising:
a FLASH controller further comprising an interface unit, an internal bus coupled to the interface unit; and a FLASH interface unit coupled to the internal bus, the FLASH interface unit includes FLASH controller logic that allows the throughput for access to a FLASH

5 memory to match the speed of the interface unit; and

6 a plurality of FLASH memories coupled to the FLASH interface unit, wherein the
7 software program for the FLASH controller is stored along with data in at least one of the
8 plurality of FLASH memories for cost reduction and field upgrade ability.

1 12. The FLASH controller of claim 11, wherein the interface unit comprises a USB
2 interface unit, wherein the USB interface unit implements a USB standard that has a bus speed
3 equal to or greater than 12 Mb/s.

1 13. The FLASH controller of claim 12 wherein the USB standard comprises the
2 USB 2.0 standard.

1 14. The FLASH controller of claim 12 wherein the throughput for access to a
2 FLASH memory to match the speed of the USB standard is accomplished by providing a wider
3 bandwidth FLASH data bus.

1 15. The FLASH controller of claim 12 wherein the throughput for access to a
2 FLASH memory to match the speed of the USB standard is accomplished by providing
3 concurrent internal and external read and write cycles.

1 16. The FLASH controller of claim 14 wherein the wider data bandwidth is
2 provided by using a FLASH memory with the appropriate data width.

1 17. The FLASH controller of claim 14 wherein the wider data bandwidth is
2 provided by using multiple FLASH memories.

1 18. The FLASH controller of claim 12 wherein the throughput for access to a
2 FLASH memory to match the speed of the USB standard is accomplished by providing a wider
3 bandwidth FLASH data bus and concurrent internal and external read and write cycles.

1 19. The FLASH controller of claim 12 including a FLASH type detection algorithm
2 for determining if a FLASH type is supported by the FLASH controller.

1 20. The FLASH controller of claim 12 wherein an external power regulator, reset
2 circuit and crystal are integrated via mixed signal technology or Multi-Chip package.

1 21. The FLASH controller of claim 11 wherein the throughput increase for access
2 to a FLASH memory is accomplished by providing a wider bandwidth FLASH data bus.

1 22. The FLASH controller of claim 11 wherein the throughput increase for access
2 to a FLASH memory is accomplished by providing concurrent internal and external read and
3 write cycles.

1 23. The FLASH controller of claim 21 wherein the wider data bandwidth is
2 provided by using a FLASH memory with the appropriate data width.

1 24. The FLASH controller of claim 21 wherein the wider data bandwidth is
2 provided by using multiple FLASH memories.

1 25. The FLASH controller of claim 11 wherein the throughput increase for access
2 to a FLASH memory is accomplished by providing a wider bandwidth FLASH data bus and
3 concurrent internal and external read and write cycles.

1 26. The FLASH controller of claim 11 including a FLASH type detection algorithm
2 for determining if a FLASH type is supported by the FLASH controller.

1 27. The FLASH controller of claim 11 wherein an external power regulator, reset
2 circuit and crystal are integrated via mixed signal technology or Multi-Chip package.